CLAIMS:

1. A semiconductor switch comprising:

two MOS transistors that are coupled in an anti-series arrangement, and a gate control circuit that is coupled to both gates of the MOS transistors, the MOS transistors being embodied as N-channel MOS transistors, both drains of the MOS transistors being interconnected, and the gate control circuit being coupled to the interconnected drains.

2. The semiconductor switch according to claim 1, the semiconductor switch further comprising a voltage limiting circuit that is coupled between the gate and the source of at least one of the MOS transistors.

3. The semiconductor switch according to claim 2, wherein the voltage limiting circuit comprises a semiconductor means.

4. The semiconductor switch according to claim 3, wherein the semiconductor means is an NMOS transistor.

5. The semiconductor switch according to claim 1, wherein the gate control circuit is arranged to perform a two phase gate pumping voltage multiplication operation.

6. The semiconductor switch according to claim 6, wherein the gate control circuit comprises a switched capacitor means.

7. The semiconductor switch according to claim 5 or claim 6, wherein the two phase gate pumping voltage multiplication operation has a tunable charge pump frequency around 15-200 KHz, preferably around 50 KHz.

8. A system comprising two electrical circuits, which system comprises a semiconductor switch according to claims 1 or 2, which semiconductor switch is interconnected between the two electrical circuits.